Course Title:	**DIGITAL ELECTRONICS**	Course Code	: 15EE34T
Semester	: **III**	Course Group	: **Core**
Teaching Scheme (L:T:P) : **4:0:0**(in Hours)		Credits	: **4 Credits**
Type of course	: **Lecture + Assignments**	Total Contact Hours	: **52**
CIE	: **25 Marks**	SEE	: **100 Marks**
Programme: Diploma in Electrical and Electronics Engg.			

Pre-requisites :	Science and Mathematics in Secondary Education and knowledge of basics of Electrical Engg.and Analog Electronics.
Course Objectives :	To introduce the concept of IC logic families, digital principles, Boolean Algebra, logic gates, combinational circuits, sequential circuits, digital interfacing, ADC, DAC and memories.

Course Topics:

Unit No	Unit Name	Hours
1	IC Logic families	4
2	Digital Principles	8
3	Boolean Algebra & Logic Gates	9
4	Combinational Logic Circuits	11
5	Sequential Logic Circuits	12
6	Digital Interfacing and Memories	8
	Total	**52**

CourseOutcomes

On successful completion of the course, the student will be able to:

1. Understand the basics of IC logic families.

2. Appraise digital principles and number system conversion.

3. Explain Logic gates and deduce the Boolean expressions using K-map.

4. Analyse different Combinational logic circuits.

5. Illustrate various Sequential logic circuits.

6. Evaluate digital interfacing and memories.

Composition of Educational Components

Questions for CIE and SEE will be designed to evaluate the various educational components (Bloom's Taxonomy) such as:

Sl. No.	Educational Component	Weightage (%)	Total Marks (Out of 145)
1	Remembering	8	10
2	Understanding	50	60
3	Application/ Analysis	42	75
	Total	**100**	**145**

Course Outcome linkage to Cognitive Level

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs
CO1	Understand the basics of IC logic families.	R/U	2, 10	4
CO2	Appraise digital principles and number system conversion.	U/A	2, 10	8
CO3	Explain Logic gates and deduce the Boolean expressions using K-map.	R/U/A	2, 10	9
CO4	Analyse different Combinational logic circuits.	U/A	2, 10	11
C05	Illustrate various Sequential logic circuits.	U/A	2, 10	12
C06	Evaluate digital interfacing and memories.	U/A	2, 10	8
		Total sessions		**52**

Course Content and Blue Print of Marks for SEE:

Unit No	Unit Name	Hour	Max. Marks per Unit	Questions to be set for (5marks) PART - A			Questions to be set for (10marks) PART - B			Marks weightage (%)
				R	U	A	R	U	A	
1	IC Logic families	4	**10**	1				0.5		7
2	Digital Principles	8	**25**		1			1	1	17
3	Boolean Algebra & Logic Gates	9	**25**	1		1		0.5	1	17
4	Combinational Logic Circuits	11	**30**		1	1		1	1	21
5	Sequential Logic Circuits	12	**35**		1	1		0.5	2	24
6	Digital Interfacing and Memories	8	**20**			1		1	0.5	14
	Total	52	145	9 (45 Marks)			10 (100 Marks)			100

Course-PO Attainment Matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
Digital Electronics	-	3	-	-	-	-	-	-	-	3

LEVEL 3- HIGHLY ADDRESSED, LEVEL 2-MODERATELY ADDRESSED, LEVEL 1-LOW ADDRESSED.
METHOD IS TO RELATE THE LEVEL OF PO WITH THE NUMBER OF HOURS DEVOTED TO THE COS WHICH ADDRESS THE GIVEN PO.
IF ≥40% OF CLASSROOM SESSIONS ADDRESSING A PARTICULAR PO, IT IS CONSIDERED THAT PO IS ADDRESSED AT LEVEL 3
IF 25 TO 40% OF CLASSROOM SESSIONS ADDRESSING A PARTICULAR PO, IT IS CONSIDERED THAT PO IS ADDRESSED AT LEVEL 2
IF 5 TO 25% OF CLASSROOM SESSIONS ADDRESSING A PARTICULAR PO, IT IS CONSIDERED THAT PO IS ADDRESSED AT LEVEL 1
If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

Course Content:

Unit –I (4 Hrs)

IC Logic families: IC logic families- definition. Definitions- threshold voltage, propagation delay, power dissipation, noise margin, logic voltage level, fan-in, fan-out, speed, operating temperature, positive and negative logic. General characteristics- TTL, ECL and CMOS, advantages and disadvantages, Definition- Tri-state logic. IC- definition, advantages of IC over discrete components.

Unit –II (8 Hrs)

Digital Principles: Definitions- bit, nibble, byte, word, and parity bit. Number system- definition, types, radix, decimal, BCD, binary and hexadecimal.BCD addition.Binary- addition, subtraction, Multiplication, Division, 1's and 2's complement. Hexadecimal- addition, subtraction, advantages. Conversion- decimal to binary and hexadecimal and vice-versa.ASCII, Gray codes, and list applications.

Unit –III (9Hrs)

Boolean Algebra & Logic Gates: Definition- Boolean variable, complement, Boolean function, expression, truth table and Buffer.Boolean Algebra- rules and laws.Logic gates NOT, AND, OR, NAND, NOR, EX-OR- definition, symbol, Boolean equation, truth table and working. De Morgan's theorems- statement and equations.Universal gates- definition, realisation of NOT, OR, AND and EXOR gates. Definitions of SOP and POS terms. Karnaugh's map up to three variables- Simplification and draw logic diagram.

Unit –IV (11 Hrs)

Combinational Logic Circuits:-definition. Adders- definition, types. Half adder- block diagram, logic diagram using AND and XOR, truth table and working. Full adder- block diagram, logic diagram using AND, OR and XOR,truth table and working.
Multiplexer- definition, block diagram. 4:1 MUX- block diagram, truth table, working, logic diagram using basic gates and applications. DeMultiplexer- definition, block diagram.1:4 DeMUX- block diagram, truth table, working, logic diagram using basic gates and applications.Seven segment display- definition, types, working and applications.
Encoders- definition, applications. Priority encoder 10 line to 4 line 74147 IC - pin diagram, truth table and working. Decoders- definition, applications. BCD to 7 segment decoder (7442 IC)- block diagram, truth table and working.

Unit –V (12 Hrs)

Sequential Logic Circuits:-definition. Definitions- level and edge triggering. Flip flops- definition, types and applications. RS flip flop and clocked RS flip flop- block diagram, truth table, logic diagram using NAND gates and working. JK flip flop- block diagram, truth table, logic diagram using NAND gates and working. Master slave JK flip flop with preset and clear input- block diagram only, truth table and working. D flip flop- block diagram,

truth table and working.Shift Registers- definition,types and applications. Four bit SISO, SIPO, PISO and PIPO shift registers using D flip flops- block diagram, truth table and operation. Counters- definition, modulus concept, timing diagram, types and applications. Four bit decade and binary asynchronous counter- block diagram using JK flip flops, truth table, timing diagramand working. Three bit synchronous up counter- block diagram, truth table, timing diagram and working.

Unit –VI (8Hrs)

Digital Interfacing and Memories: Interfacing- definition. TTL and CMOS interface-switch, LED, relay, motorand solenoid. TTL to CMOS and vice versa.ADC and DAC-definitions, types.Successive approximation ADC- block diagram and operation. Weighted Resistor DAC- block diagram and operation.Memories-definition, types, applications and working of MOS dynamic memory cell.

Reference Books:

1. Digital Fundamentals by T. L. Floyd, Pearson International Publications, Ninth Edition, 2000.
2. Electronics Principles by Malvino and Leach, Mc. Graw Hill, Third edition. 2000.
3. Modern Digital Electronics by R P Jain, Tata McGraw-Hill Education, 2003.
4. Digital Electronics: Principles and Applications by R. L. Tokheim, Tata McGraw-Hill Education, 2013.
5. Electronics Analog and Digital by I. J. Nagrath, PHI Learning Pvt. Ltd., 2013 Edition.
6. Principles of Digital Electronics by K. Meena, PHI Learning Pvt. Ltd., Fourth Printing, 2013.

e-Resources:
1. https://en.wikipedia.org/wiki/
2. https://www.google.co.in/search?sclient=psy-ab&site=&source=hp&btnG=Search&q=JK+flip+flop+using+NAND+gates
3. *www.electronics-tutorials.ws › Sequential Logic*
4. *www.circuitstoday.com/flip-flops*

Course Delivery:

The Course will be delivered through lectures, classroom interaction, animations, group discussion, exercises and student activities, assignments.

Course Assessment and Evaluation:

	What		To Whom	Frequency	Max Marks	Evidence Collected	Course Outcomes
Direct Assessment	**CIE (Continuous Internal Evaluation)**	I A Tests	Students	Three IA tests for Theory: (Average marks of Three Tests to be computed).	20	Blue Books	1 to 6
		Classroom Assignments		Student Activity	05	Report of 2 pages	1 to 6
				TOTAL	**25**		
	SEE (Semester End Examination)	End Exam	Students	End Of the Course	100	Answer Scripts at BTE	1 to 6
Indirect Assessment	Student Feedback on course		Students	Middle Of The Course	Feed Back Forms		1 to 3
	End Of Course Survey			End Of The Course	Questionnaires		1 to 6

***CIE** – Continuous Internal Evaluation   ***SEE** – Semester End Examination

Note: I.A. test shall be conducted for 20 marks. Average marks of three tests shall be rounded off to the next higher digit.

Course Contents with Lecture Schedule:

Lesson No./ Session No.	Contents	Duration
Unit I	**IC Logic families**	**4 Hours**
1.	IC logic families- definition. Definitions- threshold voltage, propagation delay, power dissipation,	01 Hour
2.	Definitions- Noise margin, logic voltage level, fan-in, fan-out, speed, operating temperature, positive and negative logic.	01 Hour
3.	General characteristics- TTL, ECL and CMOS, advantages and disadvantages,	01 Hour
4.	Definition- Tri-state logic. IC- definition, advantages of IC over discrete components.	01 Hour
Unit II	**Digital Principles**	**8 Hr**
5.	Definitions- bit, nibble, byte, word, and parity bit.	01 Hour
6.	Number system- definition, types, radix, decimal, BCD, binary and hexadecimal.	01 Hour
7.	BCD addition. Binary- addition, subtraction, Multiplication	01 Hour
8.	Binary- Division, 1's and 2's complement.	01 Hour
9.	Hexadecimal- addition, subtraction, advantages.	01 Hour
10.	Conversion- decimal to binary, decimal to hexadecimal	01 Hour
11.	Conversion- binary to decimal, binary to hexadecimal, hexadecimal to decimal,	01 Hour
12.	Conversion- hexadecimal to binary. ASCII, Gray codes, and list applications.	01 Hour
Unit III	**Boolean Algebra & Logic Gates**	**9 Hr**
13.	Definition- Boolean variable, complement, Boolean function, expression, truth table and Buffer.	01 Hour
14.	Boolean Algebra- rules and laws.	01 Hour
15.	Logic gates NOT, AND, OR- definition, symbol, Boolean equation, truth table and working.	01 Hour
16.	Logic gates NAND, NOR, EX-OR- definition, symbol, Boolean equation, truth table and working.	01 Hour
17.	De Morgan's theorems- statement and equations	01 Hour

18.	Universal gates- definition, realisation of NOT, OR gates.	01 Hour
19.	Universal gates- realisation of AND and EXOR gates.	01 Hour
20.	Definitions of SOP and POS terms. Karnaugh's map up to three variables- Simplification and draw logic diagram.	01 Hour
21.	K-map- Simplification and draw logic diagram.	01 Hour
Unit IV	**Combinational Logic Circuits**	**11 Hr**
22.	Definition. Adders- definition, types.	01 Hour
23.	Half adder- block diagram, logic diagram using AND and XOR, truth table and working.	01 Hour
24.	Full adder- block diagram, logic diagram using AND, OR and XOR,truth table and working.	01 Hour
25.	Multiplexer and DeMUX- definition, block diagram.	01 Hour
26.	4:1 MUX- block diagram, truth table, working, logic diagram using basic gates.	01 Hour
27.	1:4 DeMUX- block diagram, truth table, working, logic diagram using basic gates	01 Hour
28.	MUX and DeMUX applications. Seven segment display- definition, types and applications.	01 Hour
29.	Seven segment display- working.	01 Hour
30.	Encoders and Decoders- definition, applications.	01 Hour
31.	Priority encoder 10 line to 4 line 74147 IC - pin diagram, truth table and working.	01 Hour
32.	BCD to 7 segment decoder (7442 IC)- block diagram, truth table and working.	01 Hour
Unit V	**Sequential Logic Circuits**	**12 Hr**
33.	Sequential Logic Circuits:-definition. Definitions- level and edge triggering. Flip flops-definition, types and applications.	01 Hour
34.	RS flip flop- block diagram, truth table, logic diagram using NAND gates and working.	01 Hour
35.	Clocked RS flip flop- block diagram, truth table, logic diagram using NAND gates and working.	01 Hour
36.	JK flip flop- block diagram, truth table, logic diagram using NAND gates and working.	01 Hour
37.	Master slave JK flip flop with preset and clear input- block diagram only, truth table and working.	01 Hour
38.	D Flip flop- Block diagram, truth table and working.	01 Hour

39.	Shift Registers- definition,types and applications. Four bit SISOusing D Flip flops- block diagram, truth table and operation.	01 Hour
40.	Four bit SIPO, PISO and PIPO shift registers using D flip flops- block diagram, truth table and operation.	01 Hour
41.	Counters- definition, modulus concept, timing diagram, types and applications.	01 Hour
42.	Four bit decade asynchronous counter- block diagram using JK flip flops, truth table, timing diagramand working.	01 Hour
43.	Four bit binary asynchronous counter- block diagram using JK flip flops, truth table, timing diagramand working.	01 Hour
44.	Three bit synchronous up counter- block diagram, truth table, timing diagram and working.	01 Hour
Unit VI	**Digital Interfacing and Memories**	**8 Hr**
45.	Definitions- Interfacing. TTL to switch, LED, relay, motorand solenoid.	01 Hour
46.	CMOS to switch, LED, relay, motorand solenoid.	01 Hour
47.	TTL to CMOS and vice versa.	01 Hour
48.	ADC and DAC- definitions, types.	01 Hour
49.	Successive Approximation ADC- block diagram and operation.	01 Hour
50.	Weighted Resistor DAC- block diagram and operation.	01 Hour
51.	Memories-definition, types, applications	01 Hour
52.	Working of MOS dynamic memory cell.	01 Hour

Suggested Student Activity (any one to be submitted with 2 pages report):

1. Study and prepare a report of different IC packages and mention different scale of integration.
2. List any 2 applications with diagrams used with ASCII and Gray code each.
3. List the ICs used for different logic gates with their pin diagram details.
4. Rig up common anode 7 segment display circuit using Breadboard and IC trainer kit and display 0-9.
5. List the ICs used for Flip flops, Shift registers, Counters with their pin diagrams.
6. Prepare a report on TTL and CMOS ICwith pin diagram for interfacing Relays, Motor and Buzzer.
7. Identification and checking ICs using IC Tester.

MODEL OF RUBRICS / CRITERIA FOR ASSESSING STUDENT ACTIVITY (Course Coordinator)

Dimen sion	Scale					Students score (Group of five students)				
	1 Unsatisfactory	2 Developing	3 Satisfactory	4 Good	5 Exemplary	1	2	3	4	5
1	Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	3				
2	Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	2				
3	Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	5				
4	Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	4				
Note: Concerned faculty (Course coordinator) must devise appropriate rubrics/criteria for assessing Student activity for 5 marks One activity on any one CO (course outcome) may be given to a group of FIVE students Grand Average/Total						14/4 =3.5 ≈4				

Dimension	Scale					Students score (Five students)				
	1 Unsatisfactory	2 Developing	3 Satisfactory	4 Good	5 Exemplary	1	2	3	4	5
1.Organisation	Has not included relevant info	Has included few relevant info	Has included some relevant info	Has included many relevant info	Has included all relevant info needed	3				
2. Fulfill team's roles & duties	Does not perform any duties assigned	Performs very little duties	Performs partial duties	Performs nearly all duties	Performs all duties of assigned team roles	2				
3.Conclusion	Poor	Less Effective	Partially effective	Summarises but not exact.	Most Effective	5				
4.Conventions	Frequent Error	More Error	Some Error	Occasional Error	No Error	4				
					Total marks	14/4=3.5 ≈4				

Example only: MODEL OF RUBRICS / CRITERIA FOR ASSESSING STUDENT ACTIVITY-
Task given- Industrial visit and report writing

FORMAT OF I A TEST QUESTION PAPER (CIE)

Test/Date and Time	Semester/year	Course/Course Code	Max Marks
Ex: I test/6 th weak of sem 10-11 Am	I/II SEM		20
	Year:		

Name of Course coordinator :
Units:__ CO's:____

Question no	Question	MARKS	CL	CO	PO
1					
2					
3					
4					

Note: Internal Choice may be given in each CO at the same cognitive level (CL).

Test/Date and Time	Semester/year	Course/Course Code	Max Marks
1st Test/ 6th week, 9 Feb 16, 10-11 AM	III SEM, E & E Engg	**Digital Electronics**	20
	Year: 2015-16	Course code:	

Name of Course coordinator :
Units Covered :1 and 2
Course Outcomes : 1 and 2
Instruction :(1). Answer all questions   (2). Each question carries five marks

Question No.	Question	CL	CO	PO
1	Define IC and list the advantages of IC over discrete components. OR Define speed, logic voltage level and operating temperature	R R	1	2, 10
2	Compare the characteristics of TTL, ECL and CMOS.	U	1	2, 10
3	List the various Number systems with their radix.	U	2	2, 10
4	Add and write the result in hexadecimal i) (6E)16 and (C5)16 ii) (AC6)16 and (B59)16 OR Convert the following decimal numbers into binary equivalent i) 93 ii) 61	A A	2	2, 10

CL: Cognitive Level, R-Remember, U-Understand, A-Application, PO: Program Outcomes

Model QUESTION Paper BANK:

Course Title: DIGITAL ELECTRONICS	Course Code: 15EE34T

Unit 1 -IC Logic families

Cognitive Level: REMEMBER

1) Define IC and IC logic family.
2) Define threshold voltage, propagation delay, power dissipation.
3) Define noise margin, fan-in and fan-out.
4) Define speed, logic voltage level and operating temperature.
5) Define positive and negative logic.
6) Define Tri-state logic.
7) Define IC and list the advantages of IC over discrete components.

Cognitive Level: UNDERSTAND

8) List the characteristics of TTL, ECL and CMOS.
9) Compare the characteristics of TTL, ECL and CMOS.
10) List the advantages and disadvantages of TTL.

11)   List the advantages and disadvantages of ECL.
12)   List the advantages and disadvantages of CMOS.

Unit II - Digital Principles

Cognitive Level: UNDERSTAND

13)   Define bit, nibble, byte and word.
14)   Define parity bit and mention the importance.
15)   List the various Number systems with their radix.
16)   Explain Hexadecimal number system and list advantages.
17)   Explain briefly ASCII and Gray.

Cognitive Level: APPLICATION

18)   Add the following $(78)10 + (98)10 = (?)$ BCD.
19)   Convert the $(593)10$ to BCD.
20)   Add the binary numbers   i) 1101.101 and 111.011   ii) 11011 and1101
21)   Subtract the following   i) $(111.111)2$ from $(1010.01)2$
                                    ii) $(101)2$ from$(10110)2$
22)   Perform binary multiplication for 10.001 x 0.11 and -11101 x 100.1
23)   Perform binary division for $11001 \div 110$ and $11101.000 \div 1100$.
24)   Perform binary subtraction using 2's complement
          i) 100101 from 110011ii) 0111 from 0110
25)   Add and write the result in hexadecimal
          i) $(6E)16$ and $(C5)16$ ii)$(AC6)16$and $(B59)16$
26)   Convert the following decimal numbers into binary equivalent
          i) 93   ii) 61
27)   Convert the following decimal numbers into hexadecimal equivalent
          i) 151   ii) 498
28)   Convert the following binary numbers into decimal equivalent
          i) 01010110   ii) 110.0110
29)   Convert the following hexadecimal numbers into decimal equivalent
          2A6   ii) B2F8

Unit III- Boolean Algebra & Logic Gates

Cognitive Level: REMEMBER

30)   Define Boolean variable, complement and Buffer.
31)   Define Boolean function, expression and truth table.
32)   List rules of Boolean algebra.

Cognitive Level: UNDERSTAND

33) State De Morgan's theorems with equations.
34) Realize NOT, AND, OR and EXOR using NAND gate.
35) Realize NOT, AND, OR and EXOR using NOR gate.
36) Define SOP and POS terms.

Cognitive Level: APPLICATION

37) Explain the Commutative, Associative and Distributive laws.
38) Explain OR and NAND gates with logic diagram, Boolean function and truth table.
39) Explain NOR and EX-OR gates with logic diagram, Boolean function and truth table.
40) Explain NOT and AND gates with logic diagram, Boolean function and truth table.
41) Explain K-map method with three variables.
42) Simplify Boolean expressions using K-map and draw the logic diagram.
    $f = ABC + \overline{AB}\overline{C} + ABC + \overline{A}BC$

Unit IV - Combinational Logic Circuits

Cognitive Level: UNDERSTAND

43) Define Combinational logic circuit.
44) Define Adder and list the types.
45) Define Multiplexer. List its applications.
46) Define Multiplexer. Explain the block diagram of Multiplexer.
47) Define Encoders and list applications.
48) Define Decoders and list applications.
49) Define Encoders and Decoders.
50) Explain the working of Priority encoder.

Cognitive Level: APPLICATION

51) Explain Half adder with block diagram, truth table and logic diagram using AND and XOR gates.
52) Explain Half adder with block diagram, truth table and logic diagram.
53) Explain Full adder with block diagram, truth table and logic diagramusing AND, OR and XOR gates.
54) Explain Full adder with block diagram, truth table and logic diagram.
55) Explain the working of 4:1 MUX.
56) Explain the working of 4:1 MUX with block diagram, truth table and logic diagram.
57) Define DeMultiplexer. List its applications.
58) Explain the working of 1:4 DeMUX.
59) Explain the working of 1:4DeMUX with block diagram, truth table, and logic diagram.
60) Explain briefly Seven segment display and list the applications.
61) List and Explain the types of Seven segment display with working.
62) Explain the working of 10 line to 4 line 74147 IC with pin diagram and truth table.
63) Explain the working of BCD to 7 segment decoder (7442 IC) with block diagram and truth table.
64) Explain the working of BCD to 7 segment decoder.

Unit V- Sequential Logic Circuits

Cognitive Level: UNDERSTAND

65) Define Sequential Logic Circuit.
66) Define level and edge triggering.
67) Define Flip flop and list the applications.
68) Define Flip flop and list the types.
69) Define Shift Registers and list the applications.
70) List the types of Shift Registers.
71) Explain the operation of Four bit PIPO shift registers.
72) Define Counter, Mod and timing diagram.
73) List the types and applications of counters.
74) Explain the working of RS flip flop.
75) Explain the working of clocked RS flip flop.
76) Explain the working of JK flip flop.
77) Explain the working of D flip flop with block diagram and truth table.
78) Explain the operation of Four bit SISO shift register.
79) Explain the operation of Four bit SIPO shift registers using D flip flops with truth table.
80) Explain the operation of Four bit PISO shift registers using D flip flops with blockdiagram and truth table.
81) Explain the working of Three bit synchronous up counter.

Cognitive Level: APPLICATION

82) Explain the working of RS flip flop using NAND gates. Write the truth table.
83) Explain the working of clocked RS flip flop using NAND gates. Write the truth table.
84) Explain the working of clocked RS flip flop with block diagram, logic diagram and truth table.
85) Explain the working of JK flip flop using NAND gates.
86) Explain the working of JK flip flop using NAND gates with block diagram and logic diagram. Write the truth table.
87) Explain the working of JK flip flop Master slave using NAND gates with block diagram and truth table.
88) Explain the working of four bit decade asynchronous counter.
89) Explain the working of four bit decade asynchronous counter using JK flip flops.
90) Explain the working of four bit decade asynchronous counter using JK flip flops with block diagram, truth table and timing diagram.
91) Explain the working of four bit binary asynchronous counter using JK flip flops with block diagram, truth table and timing diagram.
92) Explain the working of four bit binary asynchronous counter using JK flip flops.
93) Explain the working of Three bit synchronous up counter with block diagram, truth table and timing diagram.

Unit –VI Digital Interfacing and Memories

Cognitive Level: UNDERSTAND

94) Define Interfacing.
95) Define ADC and list the types.
96) Define DAC and list the types.
97) Define Memory and list the applications.
98) Define RAM, ROM, PROM, EPROM, EEPROM, and flash E2PROM.
99) List the types of Memories.

Cognitive Level: APPLICATION

100) Explain TTL interfacing with switch, LED, relay, motor and solenoid.
101) Explain CMOS interfacing with switch, LED, relay, motor and solenoid.
102) Explain TTL to CMOS interface.
103) Explain CMOS to TTL interface.
104) Explain the operation of Successive approximation ADC with block diagram.
105) Explain the operation of Successive approximation ADC.
106) Explain the operation of Weighted Resistor DAC.
107) Explain the operation of Weighted Resistor DAC with block diagram.
108) Explain the working of dynamic MOS memory cell.

Model Question Paper:

Code:15EE34T

DIGITAL ELECTRONICS

III Semester Examination
Diploma in Electrical and Electronics Engg.

Time: 3 Hours
Max Marks: 100

Note: i) Answer any SIX questions from PART - A. Each question caries 5 marks.
      ii) Answer any SEVEN Questions from PART - B. Each question caries 10 marks.

PART – A

1) Define threshold voltage, propagation delay, power dissipation.
2) Convert the following decimal numbers into hexadecimal equivalent
   i) 151   ii) 498
3) State De Morgan's theorems with equations.
4) DefineMultiplexer. List itsapplications.
5) Explain the working of RS flip flop.
6) List the types of Shift Registers.
7) Explain the operation of Four bit PIPO shift registers.
8) Explain CMOS to TTL interface.
9) Define Digital to Analog Converter and list the types.

PART – B

10) (a)	List the characteristics of TTL, ECL and CMOS.	(7 M)
(b)	Explain briefly ASCII and Gray	(3 M)
11) (a)	Add the binary numbers i) 1101.101 and 111.011	(5 M)
	ii) 11011 and1101	
(b)	Convert the following decimal numbers into hexadecimal equivalent i) 151 ii) 498	(5 M)
12) (a)	Explain OR and NAND gates with logic diagram, boolean function and truth table.	(6 M)
(b)	Define Boolean variable and Buffer.	(4 M)
13) (a)	Simplify Boolean expressions using K-map and draw the logic diagram. $f = ABC + \overline{ABC} + ABC + \overline{A}BC$	(7 M)
(b)	Define SOP and POS terms.	(3 M)
14) (a)	Define Adder and list the types	(4 M)
(b)	Explain Half adder with block diagram, truth table and logic diagram.	(6 M)
15) (a)	Explain the working of 4:1 MUX.	(4 M)

(b)	Define level and edge triggering.	(6 M)
16) (a)	List and Explain the types of Seven segment display with working.	(7 M)
(b)	Define Decoders and list applications.	(3 M)
17) (a)	Explain the working of JK flip flop with block diagram and logic diagram. Write the truth table.	(7 M)
(b)	Define counter and list types.	(3 M)
18) (a)	Explain the working of fourbit binary asynchronous counter.	(5 M)
(b)	Explain TTL interfacing with switch and LED.	(5 M)
19) (a)	Explain the operation of Weighted Resistor DAC.	(3 M)
(b)	Explain the working of dynamic MOS memory cell.	(7 M)