Department of Technical Education

DIPLOMA COURSE IN ELECTRONICS AND COMMUNICATION ENGINEERING

Fifth Semester

Subject: VHDL Programming

Contact Hours/Week : 04 **Contact Hours/Semester : 64**

CONTENTS **No. Of Hrs.**

TOPIC ANALYSIS

SL. No	Major Topics	Hours Allotted
	UNIT-I	
1	**Introduction to HDL**	05
2	**Basic Language Elements**	06
3	**Behavioral Modeling**	08
	UNIT-II	
3	**Dataflow Modeling**	06
4	**Structural Modeling**	10
5	**Switch-Level Modeling**	07
	UNIT-III	
6	**Procedures and Functions**	08
7	**Mixed-Type Modeling**	07
8	**Introduction to VERILOG HDL**	03
	Tests and revision	04
	Total	**64**

GENERAL EDUCATIONAL OBJECTIVES:

1. Know what is Hardware Description Language (HDL).

2. Study the Structure of HDL Module.

3. Study different types of Descriptions .

4. Write simple HDL modules using different types of Descriptions.

5. Know Verilog briefly.

DETAILS OF COURSECONTENTS:

1. INTRODUCTION TO HDL

What is HDL, VHDL, Basic terminology-entity declaration, Architecture Body, Configuration declaration, package declaration, package body. Styles of Modeling (Descriptions), Simulation

2. **BASIC LANGUAGE ELEMENTS**

Identifiers, operators, data objects and types

3. BEHAVIORAL MODELING

Structure- Entity Declaration, Architecture Body . Variable assignment statement, sequential statements-if, signal & variable assignment, case, loop, exit, Next, assertion, report statements. Exercises

4. DATA-FLOW MODELING

Structure, signal declaration and assignment, concurrent signal assignment, constant declaration and assignment, assigning a delay time to signal assignment statement, conditional signal assignment statement, selected signal assignment statement. Data type-vectors. Exercises

5. STRUCTURAL MODELING

Organization of the structural description (Text-2), component declaration, Component Instantiation (text-1)binding, generic statement Exercises (text-2)

6. **SWITCH-LEVEL MODELING**

Definitions , Switch level description of primitive gates- inverter, two-Input AND, OR, NAND, NOR gates. Switch level description of simple Combinational logic & sequential circuits.

7. PROCEDURES AND FUNCTIONS

Description of Procedure and Tasks. Examples on Procedure and tasks.

8. MIXED-TYPE MODELING

Learn how to use different types of descriptions to write HDL modules, user defined types, VHDL Packages, implementation of arrays with examples.

9. INTRODUCTION TO VERILOG HDL

Brief history and structure of the Verilog module, Verilog operators and data types, Brief comparison of VHDL and Verilog

SPECIFIC INSTRUCTIONAL OBJECTIVES:

1. **INTRODUCTION TO HDL**
   1.1 Introduction to HDL, Structure of HDL Module ,
   1.2 Describe the Primary constructs or design units of VHDL- Entity declaration, Architecture body, Configuration declaration, Package declaration, Package body
   1.3 Study different Styles of Modeling (Descriptions)- Behavioral, Structure, Switch-Level, Data-Flow, Mixed-Type, Mixed-Language
   1.4 To know the process of Simulation.
   (refer text 1 & 2)
2. **BASIC LANGUAGE ELEMENTS**
   2.1 To study Identifiers and its types
   2.2 To know Data objects- declarations- constant, variable, signal, file and other ways to declare objects.
   2.3 To learn different Data types
      2.3.1 Scalar types- Bit, Boolean, Integer, Real, character, Physical, User defined, severity
      type
      2.3.2 Composite types- Bit-vector, Array, Record
      2.3.3 Access Types
      2.3.4 File Types
      2.3.5 Other Types- Std_Logic, Std_logic_vector, Signed, Unsigned
      (refer text 1)

3. **BEHAVIORAL MODELING**
   3.1 To know the Structure of HDL Behavioral Description
      3.1.1 Entity Declaration
      3.1.2 Architecture Body
         a. Identify the basic statements and components of behavioral Description
            i. Variable assignment statement
            ii. sequential statements- if, else-if, if-else statements , signal & variable assignment Statement, Case, Loop, exit, next, Assertion, Report Statements.
         b. Simple example programs on above statements
         (refer texts 1 & 2)

4. **DATA-FLOW MODELING**
   4.1 To know the Structure of Data-Flow Description (refer text 2)
   4.2 Identify the basic statements and components - signal declaration and assignment, concurrent signal assignment, Concurrent verses Sequential Signal Assignment, constant declaration and assignment, assigning a delay time to signal assignment statement , conditional signal assignment, selected signal assignment . (refer text 1 & 2)
   4.3 Data type-vectors (refer text 2)

4.4 Understand the fundamentals of some digital logic systems- half adder, 2x1 multiplexer, 2-bit comparator, D-latch, ripple carry adder and carry look ahead adder (refer text 2)

5. STRUCTURAL MODELING

5.1 To study the Organization of the structural description (refer text2)
5.2 To understand Component Declaration and Component Instantiation (refer text 1)
5.3 To understand Binding- Binding between Entity and Architecture, Binding between Library and Module, Binding between a Library and Component (refer text 2)
5.4 Understand the fundamentals of digital logic design for digital systems – adders, multiplexers, decoders, comparators, encoders, latches, flip-flops, and S-RAM memory cell. (refer text 2)
5.5 To know what is generic statement and its declaration

6. **SWITCH-LEVEL MODELING**

6.1 To implement Switch level description of primitive gates
  6.1.1 Inverter
  6.1.2 Two-Input AND, OR, NAND, NOR gates.
6.2 Switch level description of simple Combinational logic – Y= Not (abc +de), XNOR gate, 2x1 multiplexer
6.3 Switch level description of simple sequential circuit- SR-latch
(refer Text 2)

7. PROCEDURES AND FUNCTIONS

7.1 To study the concept of Subprograms. Types of subprograms
  7.1.1 Procedures
  7.1.2 Functions
7.2 Declaration of Subprogram
7.3 Subprogram Over loading.
7.4 Operator Over loading.
7.5 Examples on Procedure- VHDL Description of Full adder, N-Bit Ripple-Carry Adder, Unsigned Binary to an Integer, Unsigned Integer to Binary, Integer to Signed Binary.
7.6 Examples on Functions –VHDL Function to find the greater of Two signed numbers, to calculate a XOR b.
(refer Text 1 for 7.1, 7.2, 7.3 & 7.4, and Text 2 for 7.5 & 7.6)

8. MIXED-TYPE DESCRIPTIONS

8.1 Why Mixed-Type Description?
8.2 To Know VHDL user defined types
8.3 VHDL Packages
8.4 Implementation of arrays
  8.4.1 Single-Dimensional Arrays- Finding the Greatest Element of an Array,
  8.4.2 Two-Dimensional Arrays- Addition of Two Matrices
8.5 HDL Description of an ALU, 16x8 SRAM
(refer Text 2)

9. INTRODUCTION TO VERILOG HDL

9.1 Brief history and structure of the Verilog module

9.2 To study Verilog operators and data types

9.3 Brief comparison of VHDL and Verilog

(refer Text 2)

Text Books:

1. **VHDL Primer –** J. Bhaskar , Pearson Education
2. **HDL PROGRAMMING VHDL and Verilog** – Nazeih M . Botros, Dreamtech Press, New Delhi

Refernces:

1 **VHDL Programming By**: K Shashidhar, Sapna Publications..
2. **Design through Verilog HDL** –T R Padmanabhan & B Bala Tripura Sundari, Wiley India Pvt. Ltd.
3. **VHDL Programming by Example, 4th Edition** - Douglas L. Perry , Tata McGraw-Hill
4. **IEEE Standard VHDL Language reference Manual** - IEEE Std 1076, 2000 Edition-(E-book)

VHDL Programming

Model Question Paper

Time : 3 Hours **Max . Marks: 100**

Instructions: (1) Section-I is compulsory

(2) Answer any **two** full questions from each of the remaining sections

SECTION –I

1(a) Fill in the Blanks 5 X 1 = 5

(i) The signal assignment operator <= is implemented to assign a value to a signal in ----------

(ii) ---------- can have more than one input but only one output

(iii) Access data types in VHDL are similar to ---------- to objects of other types

(iv) The Std_Logic type has ---------values

(v) If two or more subprograms have same name, then the subprogram name is said to be ------

(b) Give the brief comparison between VHDL and Verilog. 5

SECTION-II

2 (a) Explain the declaration of an Entity using example 5

(b) Explain the Structural style & Behavioral Styles of Modeling's in VHDL 10

3(a) List and briefly explain different classes of Data Objects 6

(b) Define Identifiers and its types the different types 4

(c) Explain an Enumeration type of data declaration with example 5

4(a) Explain the Architectural body in Behavioral Modeling. 5

(b) Explain the Case statement with example 4

(c) Write a VHDl program for 2x1 multiplexer using ELSE-IF statement 6

SECTION-III

5(a) Differentiate Concurrent and Sequential signal assignment statements 5

(b) Write a VHDL program for 3-bit Ripple –Carry Adder 10

6(a) What is meant by Binding. 2

(b) Explain the binding between Entity and Architecture in VHDL 8

(c) Write the Structural Description for Half Adder. 5

7(a) Write the Switch level description of Two-input NAND gate 8

(b) Write the VHDL code for the logic Y= abc+de 7

SECTION-IV

8(a) Explain the different kinds of subprograms 3

(b) What is meant by operator overloading? Explain with an example 6

(c) Write a VHDL function to find the greater of two signed numbers. 6

9(a) Write a VHDL mixed-type description of 16x8 SRAM . 10

(b) Write a note on VHDL user defined data types. 5

10(a) If A & B are two unsigned variables, with A= 1100 and B= 1001, find the value of

i) A&&B, ii)B ror 2 iii) ~l (A) 6

(b) For the following HDL code, determine the type of description 3

```
Architecture Q1 of exercise is
 begin
   process (a,b)
     begin
        A<= B;
        Y<= B  AND C;
     end process;
end Q1
```

(c) Write a VHDL program to calculate the factorial of positive number using while loop 6

****